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Abstract

A memory device wherein a diode is serially connected to a programmable resistor and is in electrical communication with a buried digit line. An electrically conductive plug is electrically interposed between the digit line and a strapping layer, thereby creating a double metal scheme wherein the strapping layer is a second metal layer overlying metal wordlines. In a method of a first embodiment the strapping material is electrically connected to the digit line through a planar landing pad overlying the conductive plug. An insulative material is sloped to the planar landing pad in order to provide a surface conducive to the formation of the strapping material. In a method of a second embodiment diodes are formed, each having a maximum width equal to f , which is equal to the minimum photolithographic limit of the photolithographic equipment being used, and distanced one from the other along a length of the digit line by a maximum distance equal to f ; at least portions of the diodes are masked; at least a portion of an insulative material interposed between two diodes is removed to expose the buried digit line; and the conductive plug is formed in contact with the exposed portion of the buried digit line. After the formation of a programmable resistor in series with the diode a wordline is formed in electrical communication with each of the programmable resistors, and an insulative layer is formed overlying each wordline. Next an insulative spacer layer is deposited and etched to expose the conductive plug. The strapping layer is then formed overlying and in contact with the conductive plug.